

SECTION II—CLAIMS

1. (Currently Amended) A process comprising:
 - providing a wafer, the wafer comprising an inter-layer dielectric (ILD) having a feature therein, an under-layer deposited on the ILD, a barrier layer deposited on the under-layer and a conductive layer deposited on the barrier layer;
 - exposing the barrier layer;
 - placing the wafer in an electrolyte, such that at least the barrier layer is immersed in the electrolyte; and
 - applying an electrical potential between ~~the electrode and~~ the wafer and an electrode immersed in the electrolyte until at least part of the barrier layer is removed.
2. (Original) The process of claim 1 wherein the conductive layer is copper.
3. (Original) The process of claim 1 wherein the barrier layer comprises ruthenium (Ru), rhodium (Rh), tantalum (Ta), iridium (Ir), osmium (Os), or alloys thereof containing nitrogen (N), silicon (Si) or carbon (C).
4. (Original) The process of claim 1 wherein the under-layer is titanium (Ti), titanium nitride (TiN), tungsten (W), tungsten nitride (WN) or tantalum nitride (TaN).
5. (Original) The process of claim 1, further comprising removing at least a portion of the under-layer using chemical mechanical polishing (CMP).
6. (Original) The process of claim 1 wherein the electrolyte has a pH equal to or greater than 10.
7. (Original) The process of claim 6 wherein the electrolyte comprises a solution of potassium hydroxide (KOH), sodium hydroxide (NaOH), ammonium hydroxide (NH₄OH) or tetra-methyl ammonium hydroxide (TMAH).
8. (Original) The process of claim 1, further comprising adding an additive to the electrolyte.
9. (Original) The process of claim 8 wherein the additive is an oxidizer, a corrosion inhibitor, a surfactant, a buffer, a complexor, or combinations thereof.

10. (Original) The process of claim 1 wherein the electrical potential has a value equal to or greater than 0.5V with respect to the saturated calomel reference electrode.
11. (Original) The process of claim 1, further comprising removing at least a portion of the conductive layer using chemical mechanical polishing (CMP).
12. (Currently Amended) A process comprising:
 - providing a wafer, the wafer comprising an inter-layer dielectric (ILD) having a feature therein, an under-layer deposited on the ILD, and a barrier layer deposited on the under-layer, and a conductive layer deposited in the feature;
 - placing the wafer in an electrolyte, such that at least the barrier layer is immersed in the electrolyte; and
 - applying an electrical potential between ~~the electrode and~~ the wafer and an electrode immersed in the electrolyte until at least part of the barrier layer is removed.
13. (Original) The process of claim 12 wherein the conductive layer is copper.
14. (Original) The process of claim 12 wherein the barrier layer comprises ruthenium (Ru), rhodium (Rh), tantalum (Ta), iridium (Ir), osmium (Os), or alloys thereof containing nitrogen (N), silicon (Si) or carbon (C).
15. (Original) The process of claim 12 wherein the under-layer is titanium (Ti), titanium nitride (TiN), tungsten (W), tungsten nitride (WN) or tantalum nitride (TaN).
16. (Original) The process of claim 12, further comprising removing at least a portion of the under-layer using chemical mechanical polishing (CMP).
17. (Original) The process of claim 12 wherein the electrolyte has a pH equal to or greater than 10.
18. (Original) The process of claim 17 wherein the electrolyte comprises a solution of potassium hydroxide (KOH), sodium hydroxide (NaOH), ammonium hydroxide (NH₄OH) or tetra-methyl ammonium hydroxide (TMAH).
19. (Original) The process of claim 12, further comprising adding an additive to the electrolyte.

20. (Original) The process of claim 19 wherein the additive is an oxidizer, a corrosion inhibitor, a surfactant, a buffer, a complexor, or combinations thereof.
21. (Original) The process of claim 12 wherein the electrical potential has a value equal to or greater than 0.5V with respect to the saturated calomel reference electrode.
22. (Original) The process of claim 12, further comprising removing at least a portion of the conductive layer using chemical mechanical polishing (CMP).
- 23.-33. (Withdrawn)
34. (New) A process comprising:
- providing a wafer, the wafer comprising an inter-layer dielectric (ILD) having a feature therein, an under-layer deposited on the ILD, a barrier layer deposited on the under-layer and a conductive layer deposited on the barrier layer;
- exposing the barrier layer; and
- electrolytically removing at least part of the barrier layer.
35. (New) The process of claim 34 wherein the conductive layer is copper.
36. (New) The process of claim 34 wherein the barrier layer comprises ruthenium (Ru), rhodium (Rh), tantalum (Ta), iridium (Ir), osmium (Os), or alloys thereof containing nitrogen (N), silicon (Si) or carbon (C).
37. (New) The process of claim 34 wherein the under-layer is titanium (Ti), titanium nitride (TiN), tungsten (W), tungsten nitride (WN) or tantalum nitride (TaN).
38. (New) The process of claim 34, further comprising removing at least a portion of the under-layer using chemical mechanical polishing (CMP).
39. (New) The process of claim 34 wherein the electrolyte has a pH equal to or greater than 10.
40. (New) The process of claim 39 wherein the electrolyte comprises a solution of potassium hydroxide (KOH), sodium hydroxide (NaOH), ammonium hydroxide (NH₄OH) or tetramethyl ammonium hydroxide (TMAH).
41. (New) The process of claim 34, further comprising adding an additive to the electrolyte.

42. (New) The process of claim 41 wherein the additive is an oxidizer, a corrosion inhibitor, a surfactant, a buffer, a complexor, or combinations thereof.
43. (New) The process of claim 34 wherein the electrical potential has a value equal to or greater than 0.5V with respect to the saturated calomel reference electrode.
44. (New) The process of claim 34, further comprising removing at least a portion of the conductive layer using chemical mechanical polishing (CMP).